



1. SCOPE

The Smartceiver AU5688N1 is low cost versatile serial signal to parallel signal converter.

2. OUTLINE

See Fig.1 below.

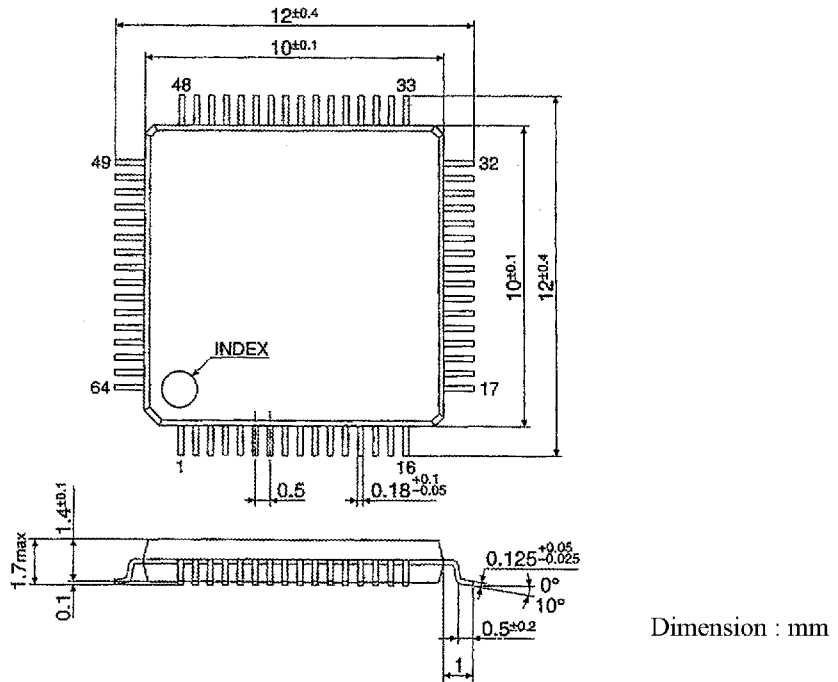


Fig. 1

3. FUNCTION

The single chip converter has 2 types of serial to parallel conversion format that is format A and format B. In addition, format A has 2 modes that is I frame mode and II frame mode. Format B has II frame mode only. See table I below.

TABLE I

PIN #	SYMBOL	FORMAT A			FORMAT B		
		I FRAME MODE	II FRAME MODE		II FRAME MODE		
			Data 1	Data 2	Data 1	Data 2	Data 3
60	A0	L	L	L	H	H	H
1	A1	L	H	H	H	H	H
13	$\overline{\text{CSPD}}^*$	×	L	L	L	L	L
3	SEL 1 <sub>PD</sub> <sup>*</sup>	×	L	H	L	L	H
5	SEL 2 <sub>PD</sub> <sup>*</sup>	×	×	×	L	H	L
ENCODER APPLICATION		TS5643N50, N150 etc.			TS5640N353 etc.		

Notes : (1) <sub>PD</sub> : With pull down resistor.

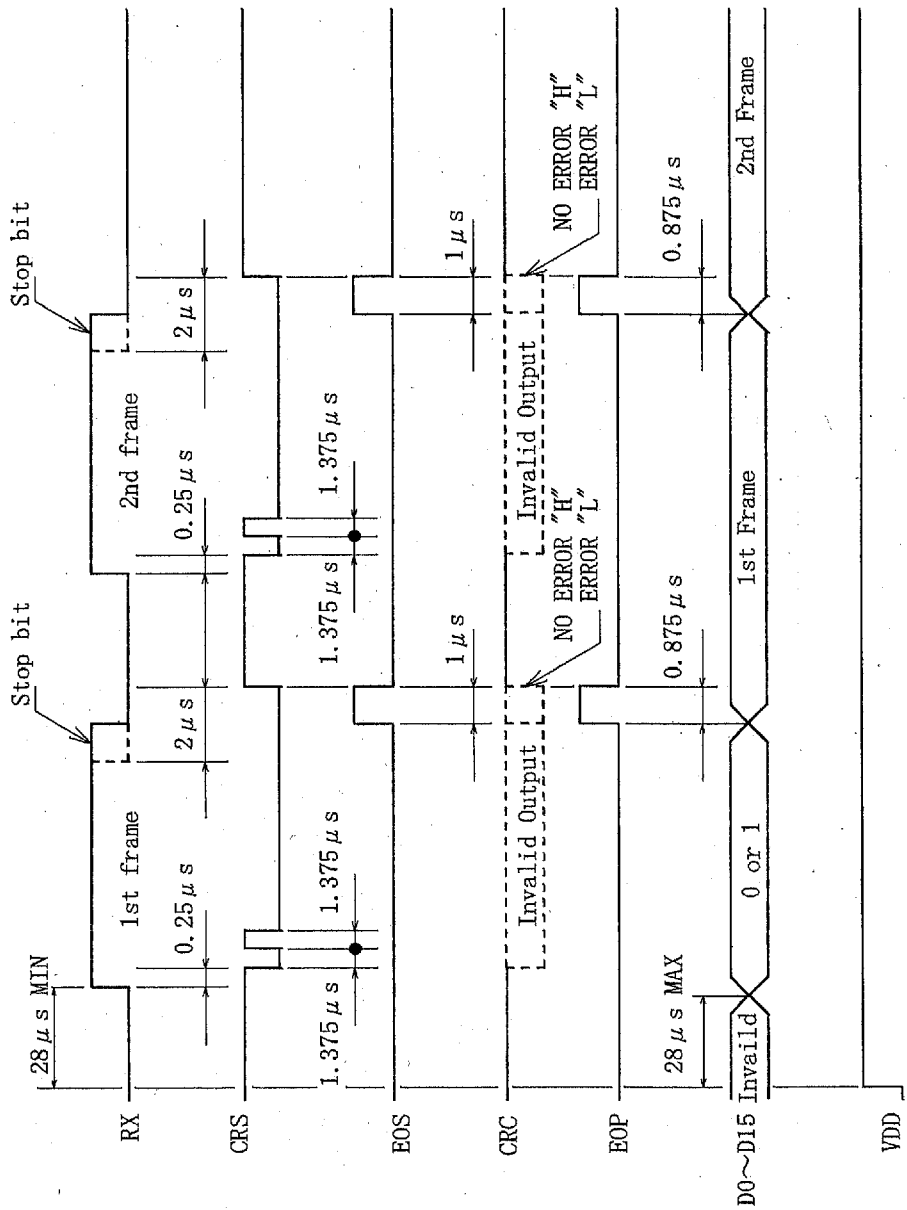
(2) × : Don't care. Logical L recommended.

DWG NO.	3	4	5	6	7	8	9	10	11	12	SHEET
S P C 0 0 4 7 0 6 Y 0 0											2 /

4. TIMING DIAGRAMS

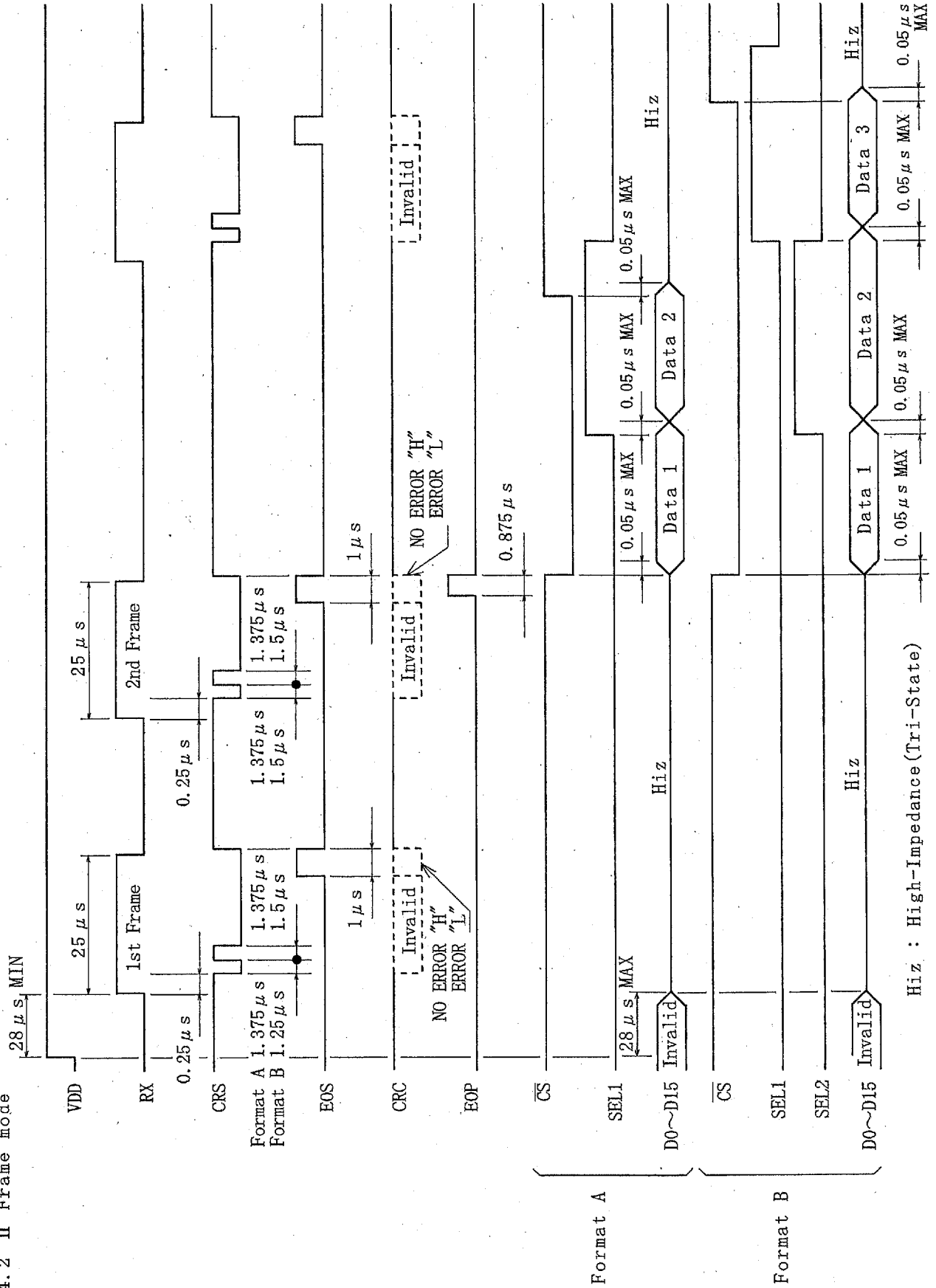
- (1) Global clock : 8MHz
- (2) Bit rate : 1Mbps
- (3) Timing tolerance :  $\pm 0.125 \mu s$

4.1 I Frame mode



DWG NO.	3	4	5	6	7	8	9	10	11	12	SHEET	
	S	P	C	0	0	4	7	0	6	Y	0	0
											3	

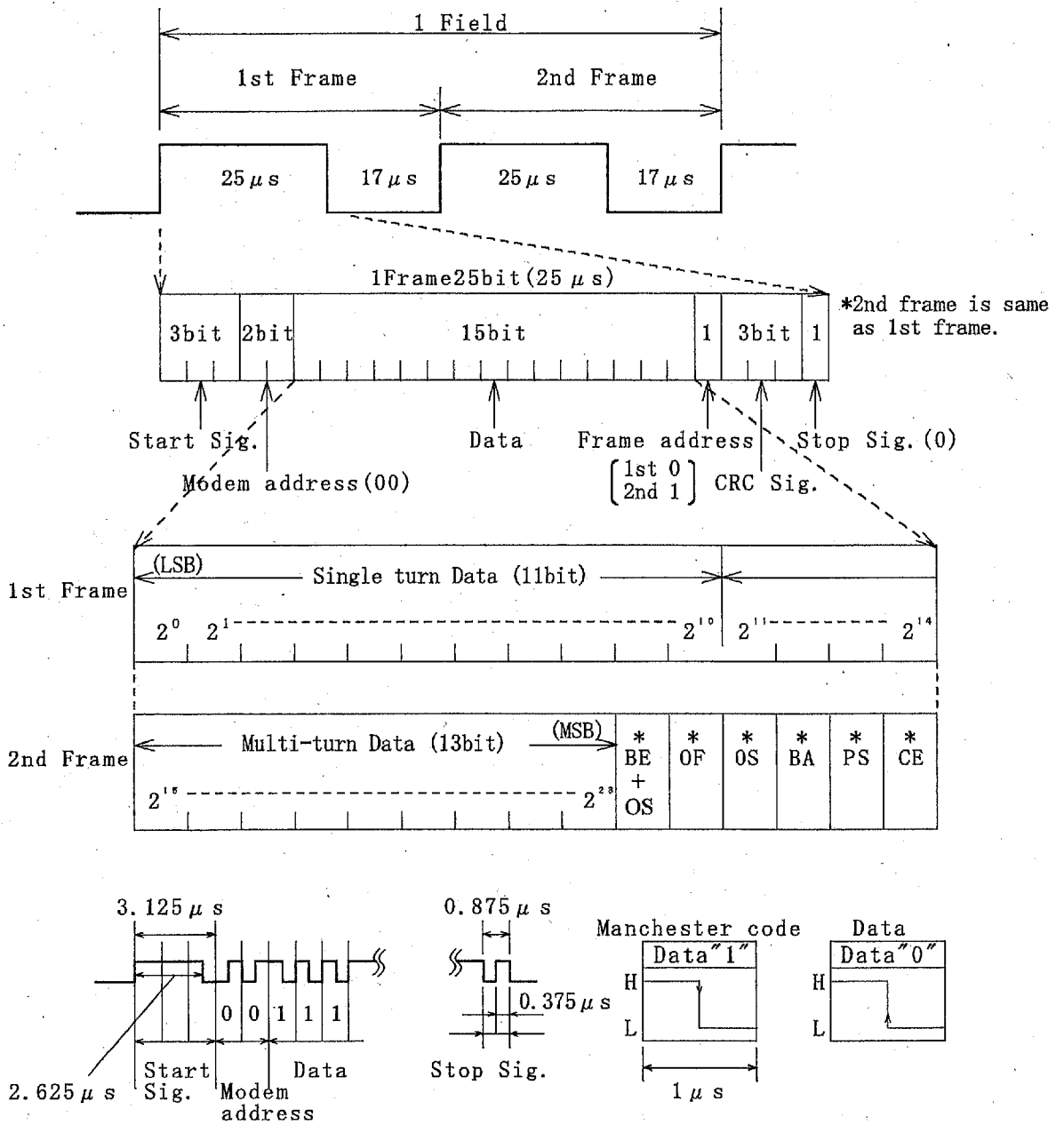
4.2 II Frame mode



Hiz : High-Impedance (Tri-State)

5. SERIAL SIGNAL FORMAT

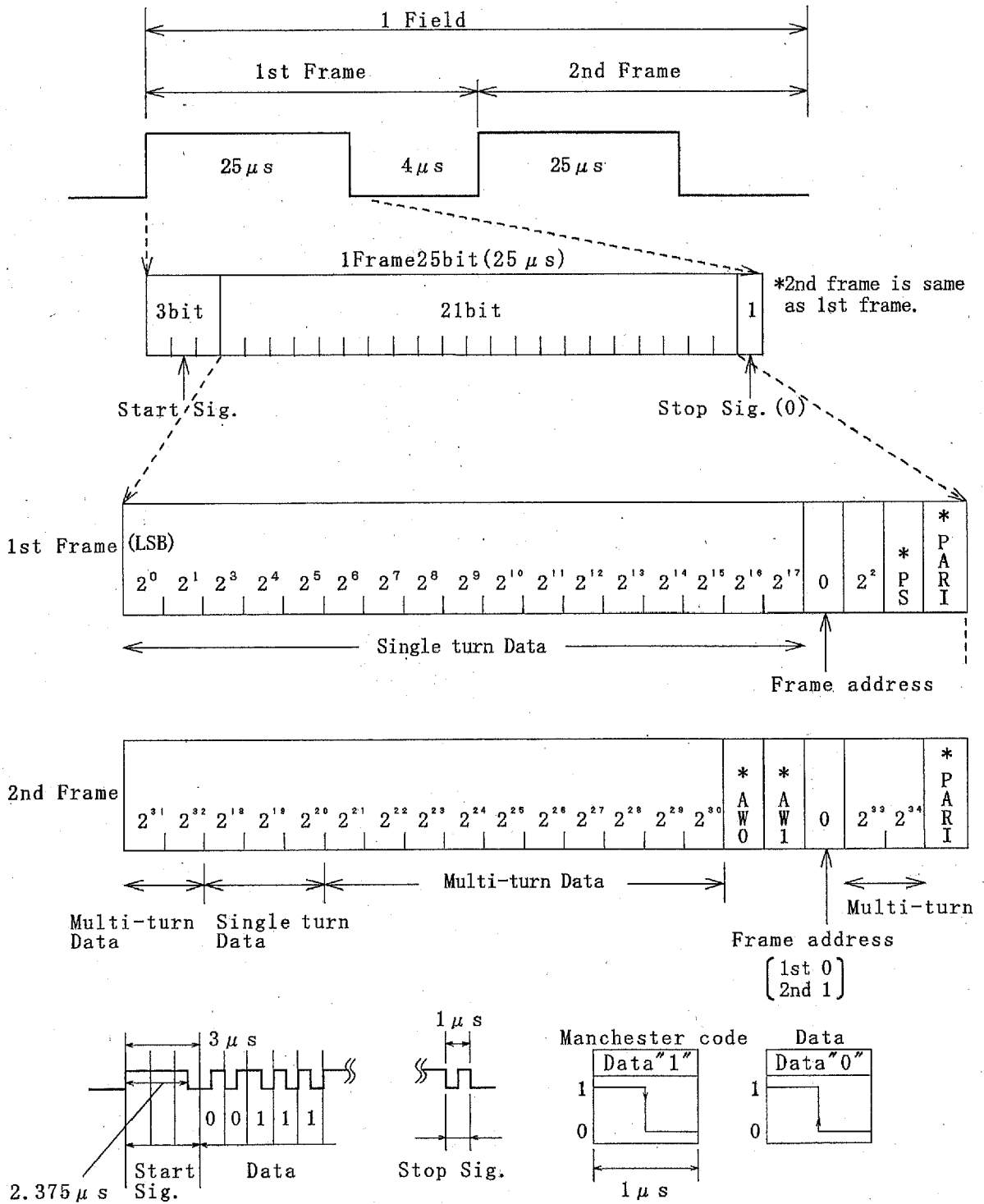
(1) FORMAT A



\* BE;OF;OS;BA;PS;CE : See encoder (TS5643N100) spec. sheets.

DWG NO.	3	4	5	6	7	8	9	10	11	12	SHEET
S P C 0 0 4 7 0 6 Y 0 0											5 /

(2) FORMAT B



\* PS;PARI;AW0;AW1 : See encoder(TS5640N353) spec. sheets.

DWG NO.	3	4	5	6	7	8	9	10	11	12	SHEET
S P C 0 0 4 7 0 6 Y 0 0											6 /

6. OUTPUT SIG. FORMAT.

Format	Frame	Data select		Data																		
		CS	SEL1	SEL2	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15		
Format A Encoder TS5643N100	Data 1	L	L	X	Single turn Data. (11bit)											Frame address						
					LSB	$2^0$	$2^1$	$2^2$	$2^3$	$2^4$	$2^5$	$2^6$	$2^7$	$2^8$	$2^9$	$2^{10}$	MSB	LSB	$2^{11}$	$2^{12}$	$2^{13}$	$2^{14}$
Format B Encoder TS5640N353	Data 2	L	H	X	Multi-turn Data. (13bit)											Frame address						
						$2^{15}$	$2^{16}$	$2^{17}$	$2^{18}$	$2^{19}$	$2^{20}$	$2^{21}$	$2^{22}$	$2^{23}$	MSB	BE	OF	OS	BA	PS	CE	1
Format B Encoder TS5640N353	Data 1	L	L	L	Single turn Data. (20bit)																	
					LSB	$2^0$	$2^1$	$2^2$	$2^3$	$2^4$	$2^5$	$2^6$	$2^7$	$2^8$	$2^9$	$2^{10}$	$2^{11}$	$2^{12}$	$2^{13}$	$2^{14}$	$2^{15}$	
Format B Encoder TS5640N353	Data 2	L	L	H	Multi-turn Data. (15bit)											Frame address						
						$2^{16}$	$2^{17}$	$2^{18}$	$2^{19}$	$2^{20}$	$2^{21}$	$2^{22}$	$2^{23}$	$2^{24}$	$2^{25}$	$2^{26}$	$2^{27}$	$2^{28}$	$2^{29}$	$2^{30}$	$2^{31}$	
Format B Encoder TS5640N353	Data 3	L	H	L	Multi-turn Data. (15bit)																	
						$2^{32}$	$2^{33}$	$2^{34}$	MSB	PS	AW0	AW1	0	0	0	0	0	0	0	0	0	0

7. PIN FUNCTION

Pin Name	Pin #	Pin Type	Description
VSS	24,36, 38,46, 56	Ground	0.1 $\mu$ F decoupling capacitors must be placed between the VDD and VSS pins.
VDD	21,55	Power	Power pin.
D0	47	Output	Parallel date output. The output signals will be invalid during initial 28 $\mu$ s as maximum after turning on the power supply.
D1	45		
D2	44		
D3	43		
D4	42		
D5	41		
D6	40		
D7	39		
D8	37		
D9	34		
D10	33		
D11	31		
D12	30		
D13	29		
D14	28		
D15	27		
RST	62	Input	Reset input (active low). Fix to be high level.
CLK	61	Input	8MHz global clock input.
$\overline{\text{CS}}$	13	Input	Chip-select input (active low). The $\overline{\text{CS}}$ low logic level locks the parallel date out (D0~D15) of II frame mode.

Pin Name	Pin #	Pin Type	Description
A0	63	Input	Mode select input. See teble I.
A1	1		
SEL-1	3	Input	Mode select input. See teble I.
SEL-2	6		
Rx	26	Input	Serial date input. Bit rate : 1Mbps. Unable to receive the serial signals during initial 28 $\mu$ s as maximum after turning on the power supply.
CRS	25	Input	Carrier sense sig. Output (active low). See item 4 Timing diagrams.
EOS	51	Output	After receiving one flame serial date,EOS sig.output (active high). See item 4 Timinng diagrams.
CRC	50	Output	Cyclic Redundancy Check signal output or parity error check signal output. The CRC signal outputs at the EOS signal logical high. See item 4 Timing diagrams.
EOP	48	Output	The EOP signal is AND gated signal of EOS and CRC. Rising edge on the EOP signal presents the current parallel date output.
IA1	57	Input	A inverter input and output. See item 9.1 Global clock circuit.
IY1	58	Output	
IY2	60	Output	Clock output. See item 9.1 Global circuit.
NC	Other	-----	No nonnection.

8. CHARACTERISTICS

8.1 MAXIMUM RATINGS

(VSS = 0 [V])

Characteristic	Symbol	Rating	Unit
Power Supply	VDD	VSS -0.3~6.5	V
Input Voltage	VIN	VSS -0.3~VDD +0.5	V
Output Voltage	VOUT	VSS -0.3~VDD +0.5	V
Output Current / 1 Pin	IOUT	±24	mA
Storage Temperature Range	Tstg	-55~150	°C
Power Dissipation	PD	200	mW

8.2 RECOMMENDED OPERATING CONDITIONS

(VSS = 0 [V])

Characteristic	Symbol	MIN	TYP	MAX	Unit
Power Supply	VDD	4.5	5.0	5.5	V
Input Voltage	VIN	VSS	—	VDD	V
Operating Temperature	Topr	-20	—	85	°C

8.3 ELECTRICAL CHARACTERISTICS

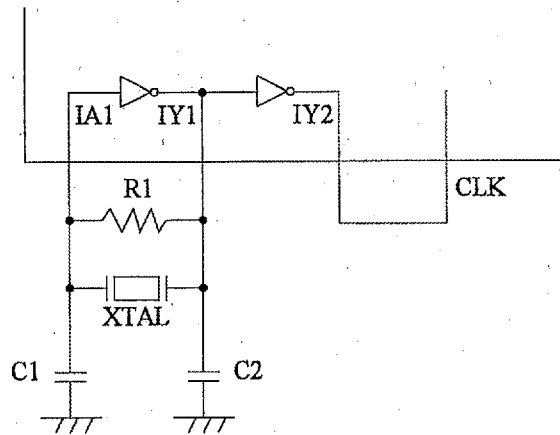
Characteristics	Symbol	Condition	MIN	TYP	MAX	Unit
Power Supply	IDD	Stillness Condition VIN = VDD or VSS IOH = IOL = 0			200	μA
Global Clock Frequency	CLK			8		MHz
Output Voltage	VOH	VDD = MIN	VDD - 0.4			V
	VOL			VSS + 0.4		V
Input Voltage	VIH	VDD = MAX	2.0			V
	VIL	VDD = MIN			0.8	V
Input Leak Current	IIL	VDD = MAX VIH = VDD IIL = VSS	-1		1	μA
Output Current	IOH	D0 ~ D15	-6.0			mA
	IOL				12.0	
	IOH	EOP,EOS,CRS,CRC	-3.0			
	IOL				6.0	

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DWG NO.	3	4	5	6	7	8	9	10	11	12	SHEET	
	S	P	C	0	0	4	7	0	6	Y	00	10 /

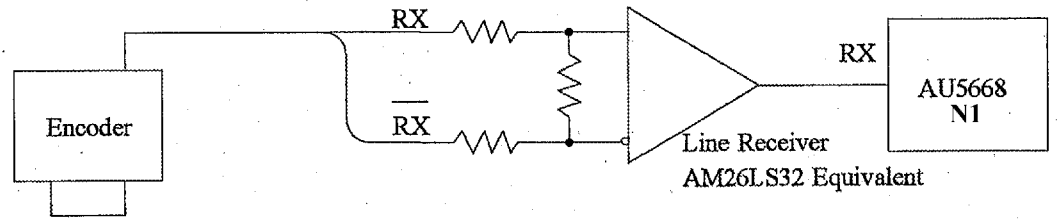
9. APPLICATION

9.1 Global Clock Circuit

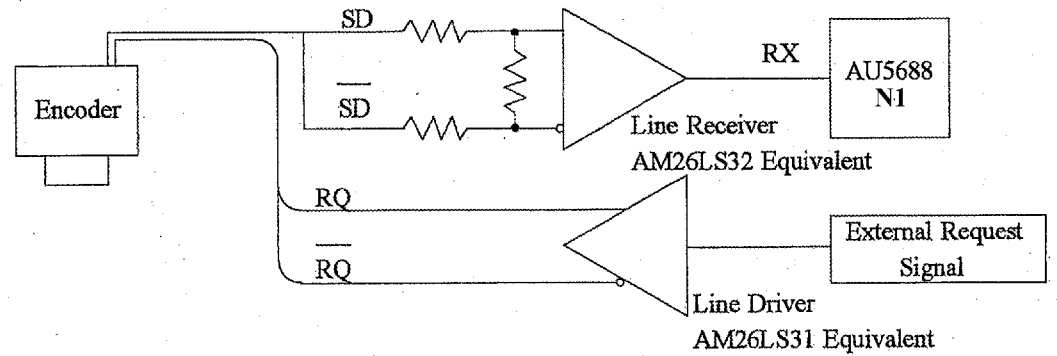


9.2 Encoder Interface

(1) TS5643N50,N150 etc. Application



(2) TS5640N353 etc. Application



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DWG NO.	3	4	5	6	7	8	9	10	11	12	SHEET
S P C 0 0 4 7 0 6 Y 0 0											11 /